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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/020,647 02/09/98 FJELSTAD

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000530  
LERNER, DAVID, LITTENBERG,  
KRUMHOLZ & MENTLIK  
600 SOUTH AVENUE WEST  
WESTFIELD NJ 07090

MMC1/0801

EXAMINER

GRAYBILL, D

ART UNIT

PAPER NUMBER

2814

DATE MAILED:

08/01/01

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

**SUPPLEMENTAL**  
**Office Action Summary**

Application No.  
**09/020,647**

Applicant(s)

**Fjelstad**

Examiner  
**David E. Graybill**

Group Art Unit  
**2814**



☒ Responsive to communication(s) filed on 4 Aug 1900

☒ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

**Disposition of Claims**

☒ Claim(s) 1-11 and 21-34 is/are pending in the application.

Of the above, claim(s) 24 is/are withdrawn from consideration.

☐ Claim(s) \_\_\_\_\_ is/are allowed.

☒ Claim(s) 1-11, 21-23, and 25-34 is/are rejected.

☐ Claim(s) \_\_\_\_\_ is/are objected to.

☐ Claims \_\_\_\_\_ are subject to restriction or election requirement.

**Application Papers**

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.

☒ The proposed drawing correction, filed on 27 Jul 1900 is ☒ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some\* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) \_\_\_\_\_

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\*Certified copies not received: \_\_\_\_\_

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

**Attachment(s)**

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). \_\_\_\_\_

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

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In view of the papers filed 8-4-00, it has been found that this nonprovisional application, as filed, through error and without deceptive intent, improperly set forth the inventorship, and accordingly, this application has been corrected in compliance with 37 CFR 1.48(a). The inventorship of this application has been changed by addition of Konstantine Karavakis as a named inventor.

The application will be forwarded to the Office of Initial Patent Examination (OIPE) for issuance of a corrected filing receipt, and correction of the file jacket and PTO PALM data to reflect the inventorship as corrected.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was

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made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-4, 6, 7, 11, 21-23, 25-30, 33 and 34 are rejected under 35 U.S.C. 102(b) as anticipated by Kwon (5070297) or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kwon (5070297).

At column 4, line 13 to column 7, line 34, Kwon teaches:

1. A method of creating a compliant semiconductor chip package assembly comprising the steps of providing a first dielectric protective layer 34 on a contact bearing surface of a semiconductor chip 14, wherein the semiconductor chip has a central region bounded by chip contacts 36 of the semiconductor chip and wherein the dielectric protective layer has a plurality of apertures such that the chip contacts are exposed; providing a compliant layer 32 atop the first dielectric protective layer within the central region, wherein said compliant layer has a substantially flat top surface, a bottom surface that is attached to the first dielectric protective layer and sloping edges between the top surface and the bottom surface; and selectively electroplating elongated bond ribbons 28 atop the first dielectric protective layer and the compliant layer wherein each bond ribbon electrically connects each chip contact to a respective conductive terminal 20-22-24 on the top surface of the compliant layer, and wherein said elongated bond ribbons extend along the sloping edges of said compliant layer.

2. The method according to Claim 1 further including the step of providing a second dielectric protective layer 26 atop exposed assembly elements 28 on the terminal side of the assembly after

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the step of selectively electroplating the bond ribbons, wherein the second dielectric protective layer has a plurality of apertures such that the terminals are exposed.

3. The method according to Claim 1 wherein the compliant layer material is selected from the group consisting of silicone, flexibilized epoxy, a thermosetting polymer, fluoropolymer, thermoplastic polymer, polyimide, foams and combinations or composites thereof.
4. The method according to Claim 1 further including the step of providing for an encapsulant layer 26 atop an exposed surface of the bond ribbons.
6. The method according to Claim 4 further including the step of providing for a second dielectric protective layer 21 atop the encapsulant layer wherein the second dielectric protective layer has a plurality of apertures such that terminal positions are exposed.
7. The method according to Claim 1 wherein a silicon dioxide passivation layer on the face surface of the semiconductor chip comprises the first dielectric protective layer.
11. The method according to Claim 1 wherein the sloping edges of the compliant layer have a first transition region near the top surface of the compliant layer and a second transition region near the bottom surface of the compliant layer and wherein both the first transition region and the second transition region have a radius of curvature.
21. A method of making a compliant microelectronic assembly comprising the steps of: providing a microelectronic element 38 having a first surface and a plurality of contacts 36 disposed on the first surface thereof; providing a compliant layer 32 over the first surface of said microelectronic element, said compliant layer having a bottom surface facing toward said first surface of said

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microelectronic element, a top surface facing upwardly away from said microelectronic element and one or more edge surfaces extending between said top and bottom surfaces, and then selectively forming elongated, flexible bond ribbons 28 over said compliant layer so that said bond ribbons extend over said top surface and one or more of said edge surfaces and said bond ribbons electrically connect said contacts to conductive terminals 20-22-24 overlying the top surface of said compliant layer.

22. The method as claimed in claim 21, wherein said contacts on said microelectronic element are disposed in a first region of said first surface, said compliant layer overlies a second region of said first surface, and one or more edge surfaces include one or more border edge surfaces extending along one or more borders between said first and second regions.

23. The method as claimed in claim 21, wherein said selectively forming bond ribbons step includes selectively electroplating said bond ribbons.

25. The method as claimed in claim 21, further comprising the step of: before the providing a compliant layer step, providing a first dielectric protective layer 34 on the first surface of the microelectronic element, the first dielectric layer having a plurality of apertures therein so that said contacts are accessible therethrough, the providing the compliant layer step including the step of providing the compliant layer over said first dielectric protective layer.

26. The method as claimed in claim 25, the selectively forming flexible bond ribbons step including selectively electroplating said bond ribbons atop said first dielectric protective layer and said compliant layer.

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27. The method as claimed in claim 21, further including the step of providing a dielectric cover layer 21 over said compliant layer and said bond ribbons after the step of selectively forming the bond ribbons, wherein the cover layer has a plurality of apertures so that said terminals are accessible therethrough.

28. The method as claimed in claim 21, further including the step of providing an encapsulant layer 26 over an exposed surface of the bond ribbons.

29. The method as claimed in claim 28, further including the step of providing a second dielectric protective layer 21 atop the encapsulant layer wherein the second dielectric protective layer has a plurality of apertures so that said terminals are accessible therethrough.

30. The method as claimed in claim 21, further including the step of depositing a barrier metal 30 atop said contacts, prior to the step of forming the bond ribbons, whereby the barrier metal (inherently) helps to prevent voiding between the contacts and the bond ribbons.

33. The method as claimed in claim 21, wherein the edge surfaces of the compliant layer are sloping surfaces which extend in both vertical and horizontal directions.

34. The method as claimed in claim 33, wherein at least some of said sloping edge surfaces have first transition regions near the top surface of the compliant layer and second transition regions near the bottom surface of the compliant layer, and wherein both the first and second transition regions have respective radii of curvature.

To further clarify the teaching of forming elongated bond ribbons 28, it is noted that Kwon teaches that the contacts 28 are small and narrow in width in proportion to length or height; therefore, the contacts are elongated.

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To further clarify the teaching of first transition regions near the top surface of the compliant layer and second transition regions near the bottom surface of the compliant layer, it is noted that it is inherent that the first and second regions near the top and bottom surface, respectively, transition into neighboring regions of the compliant layer and other neighboring layers.

Although Kwon does not appear to explicitly teach a process wherein both the first and second transition regions have respective radii of curvature, it is inherent in the process of Kwon that the regions have radii equal to zero or greater.

Because applicant introduced the amendatory limitation "elongated," apparently to overcome the rejection over Kwon which was made in the previous office action and which is maintained in the instant office action, in the alternative, the claims are further rejected under 35 U.S.C. 103(a) over Kwon.

Specifically, although Kwon does not appear to explicitly teach the term "elongated," it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose this particular configuration because applicant has not disclosed that the configuration is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical, and it appears prima facie that the process would possess utility using another configuration. Moreover, it has been held that limitations directed to size and configuration are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In*



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*re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Claims 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon (5070297).

Kwon is applied as it was applied to claims 1-4, 6, 7, 11, 21-23, 25-30, 33 and 34.

As cited *supra*, Kwon teaches:

8. The method according to Claim 1 further including the step of plating a barrier metal 30 atop the semiconductor chip contacts, whereby the barrier metal (inherently) helps to prevent voiding at the boundary between the semiconductor chip contacts and the bond ribbons. However, Kwon does not appear to explicitly teach the practice of this step prior to the step of providing the compliant layer. Nonetheless, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed sequence because applicant has not disclosed that the limitation is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical. In fact, there is no support for this claim limitation elsewhere in the disclosure. Moreover, it is well established that, in a well known process, the order of performing process steps is *prima facie* obvious in the absence of new or unexpected results. *Ex parte Rubin* 128 USPQ (PO BdPatApp 1959).

Kwon also does not appear to explicitly teach:

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5. The method according to Claim 4 wherein the encapsulant layer material is selected from the group consisting of silicone, flexibilized epoxy, thermoplastic and gel. Nonetheless, as cited, Kwon teaches that "Protective coating 26 may comprise any number of compliant materials having sufficient elastic, protective, and adhesive properties for the purposes of the present invention." Furthermore, judicial notice is taken that it is well known to select protective coating encapsulant layers from the group consisting of silicone, flexibilized epoxy, thermoplastic and gel. Moreover, it would have been obvious to combine the well known process with the process of Kwon because it would provide a protective coating.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 9, 10, 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon as applied to claims 1-4, 6, 7, 11, 21-23, 25-30, 33 and 34 supra, and further in combination with Palagonia (5874782).

As cited supra, Kwon teaches:

9. The method according to Claim 1 applied simultaneously to a multiplicity of undiced semiconductor chips 14 on a wafer 10 to form a corresponding multiplicity 12 of compliant semiconductor chip packages 14.

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10. The method according to Claim 1 applied simultaneously to a multiplicity of adjacent semiconductor chips 14 arranged in an array to form a corresponding multiplicity 12 of compliant semiconductor chip packages 14.

31. The method as claimed in claim 21, the method being applied to a plurality of undiced semiconductor chips 14 on a wafer 10 to form a corresponding plurality 12 of compliant semiconductor chip packages 14.

32. The method as claimed in claim 21, the method being applied to a plurality of adjacent semiconductor chips 14 arranged in an array to form a corresponding multiplicity 12 of compliant semiconductor chip packages 14.

However, Kwon does not appear to explicitly teach:

9. The method further including the step of dicing the packages following the step for selectively electroplating the bond ribbons.

10. The method further including the step of dicing the packages following the step for selectively electroplating the bond ribbons.

31. The method further including the step of separating the packages following the step of depositing the bond ribbons.

32. The method further including the step of separating the packages following the step of selectively electroplating the bond ribbons.

Nevertheless, Palagonia teaches a method including a step of dicing and separating a plurality of adjacent compliant semiconductor chip packages 22 arranged in an array on a wafer 20 following a step of selectively electroplating bond ribbons 26. Moreover, it would have been

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obvious to combine the process of Palagonia with the process of Kwon because it would facilitate testing of individual chips.

Applicant's amendment and remarks filed 8-4-00 are addressed in the rejection supra and are further addressed infra.

Applicant contends that Kwon does not teach "wherein elongated bond ribbons extend along the sloping edges of said compliant layer." This contention is respectfully traversed because Kwon explicitly teaches that the ribbons 28 are "V-shaped," and further illustrates that the V-shaped ribbons are small and narrow in width in proportion to length or height along the sloping edges of compliant layer 32.

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

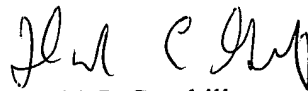
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

**Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to the Customer Service Office, TC 2800, 703/306-3329.**

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Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m..

The fax phone number for group 2800 is (703)305-3431.



David E. Graybill  
Primary Examiner  
Art Unit 2814

D.G.